WHAT IS CLAIMED IS:

1. An image sensor array apparatus, comprising:

a plurality of rows of pixel circuits, each said row including a plurality of segments having therein a plurality of said pixel circuits;

a plurality of column lines for readout of image information sensed by said pixel circuits, said pixel circuits of each said row respectively coupled to said column lines; and

a plurality of control circuits, said control circuits respectively coupled to said segments of pixel circuits, each said control circuit for resetting the pixel circuits of the corresponding segment without resetting the pixel circuits of all of the remaining segments of the corresponding row.

2. The apparatus of Claim 1, wherein each of said control circuits is further operable for permitting the pixel circuits of the corresponding segment to drive their associated column lines without requiring the pixel circuits of all of the remaining segments of the corresponding row to drive their associated column lines.

3. The apparatus of Claim 2, wherein each of said pixel circuits includes first and second control inputs, each of said control circuits coupled to said first and second control inputs of the pixel circuits of the corresponding segment.

4. The apparatus of Claim 3, wherein said first control input is a reset input which resets said pixel circuit, and wherein said second control input is a readout input which causes said pixel circuit to drive its associated column line.

5. The apparatus of Claim 4, wherein each of said control circuits includes first and second logic gates having respective outputs which are respectively coupled to said reset and readout inputs of the pixel circuits of the corresponding segment.

6. The apparatus of Claim 3, wherein each of said control circuits includes first and second logic gates having respective outputs which are respectively coupled to said first and second control inputs of the pixel circuits of the corresponding segment.

7. The apparatus of Claim 6, wherein said first and second logic gates are AND gates.

8. The apparatus of Claim 2, wherein each of said control circuits is further operable for resetting the pixel circuits of the corresponding segment without resetting the pixel circuits of any of the remaining segments of the corresponding row.

9. The apparatus of Claim 8, wherein each of said control circuits is further operable for permitting the pixel circuits of the corresponding segment to drive their associated column lines without requiring the pixel circuits of any of the remaining segments of the corresponding row to drive their associated column lines.

10. The apparatus of Claim 2, wherein each of said control circuits is further operable for permitting the pixel circuits of the corresponding segment to drive their associated column lines without requiring the pixel circuits of any of the remaining segments of the corresponding row to drive their associated column lines.

11. The apparatus of Claim 1, wherein each of said pixel circuits includes a control input, each of said control circuits coupled to said control input of the pixel circuits of the corresponding segment.

12. The apparatus of Claim 11, wherein said control input is a reset input which resets said pixel circuit.

13. The apparatus of Claim 12, wherein each of said control circuits includes a logic gate having an output which is coupled to said reset input of the pixel circuits of the corresponding segment.

14. The apparatus of Claim 11, wherein each of said control circuits includes a logic gate having an output which is coupled to said control input of the pixel circuits of the corresponding segment.

15. The apparatus of Claim 14, wherein said logic gate is an AND gate.

16. The apparatus of Claim 1, wherein each of said control circuits is further operable for resetting the pixel circuits of the corresponding segment without resetting the pixel circuits of any of the remaining segments of the corresponding row.

17. The apparatus of Claim 1, provided as a CMOS image sensor array.

18. The apparatus of Claim 1, provided on a single integrated circuit together with a compression engine coupled thereto and a memory circuit coupled to said compression engine.

19. A method of controlling an image sensor array having a plurality of rows of pixel circuits and a plurality of column lines for readout of image information sensed by the pixel circuits, comprising:

identifying within a row a plurality of segments having therein a plurality of pixel circuits; and

resetting the pixel circuits of a desired segment without resetting the pixel circuits of all of the remaining segments of the row.

20. The method of Claim 19, including the pixel circuits of the desired segment driving their associated column lines without the pixel circuits of all of the remaining segments of the row driving their associated column lines.

21. The method of Claim 20, wherein said resetting step includes resetting the pixel circuits of the desired segment without resetting the pixel circuits of any of the remaining segments of the row.

22. The method of Claim 21, wherein said driving step includes the pixel circuits of the desired segment driving their associated column lines without the pixel circuits of any of the remaining segments of the row driving their associated column lines.

23. The method of Claim 20, wherein said driving step includes the pixel circuits of the desired segment driving their associated column lines without the pixel circuits of any of the remaining segments of the row driving their associated column lines.

24. The method of Claim 19, wherein said resetting step includes resetting the pixel circuits of the desired segment without resetting the pixel circuits of any of the remaining segments of the row.

25. The method of Claim 19, including resetting an m x n block of the pixel circuits without resetting any of the remaining pixel circuits, including resetting the pixel circuits of m segments which have n-pixels each and which are respectively located at corresponding locations in m rows of the array.